0627T 0525260

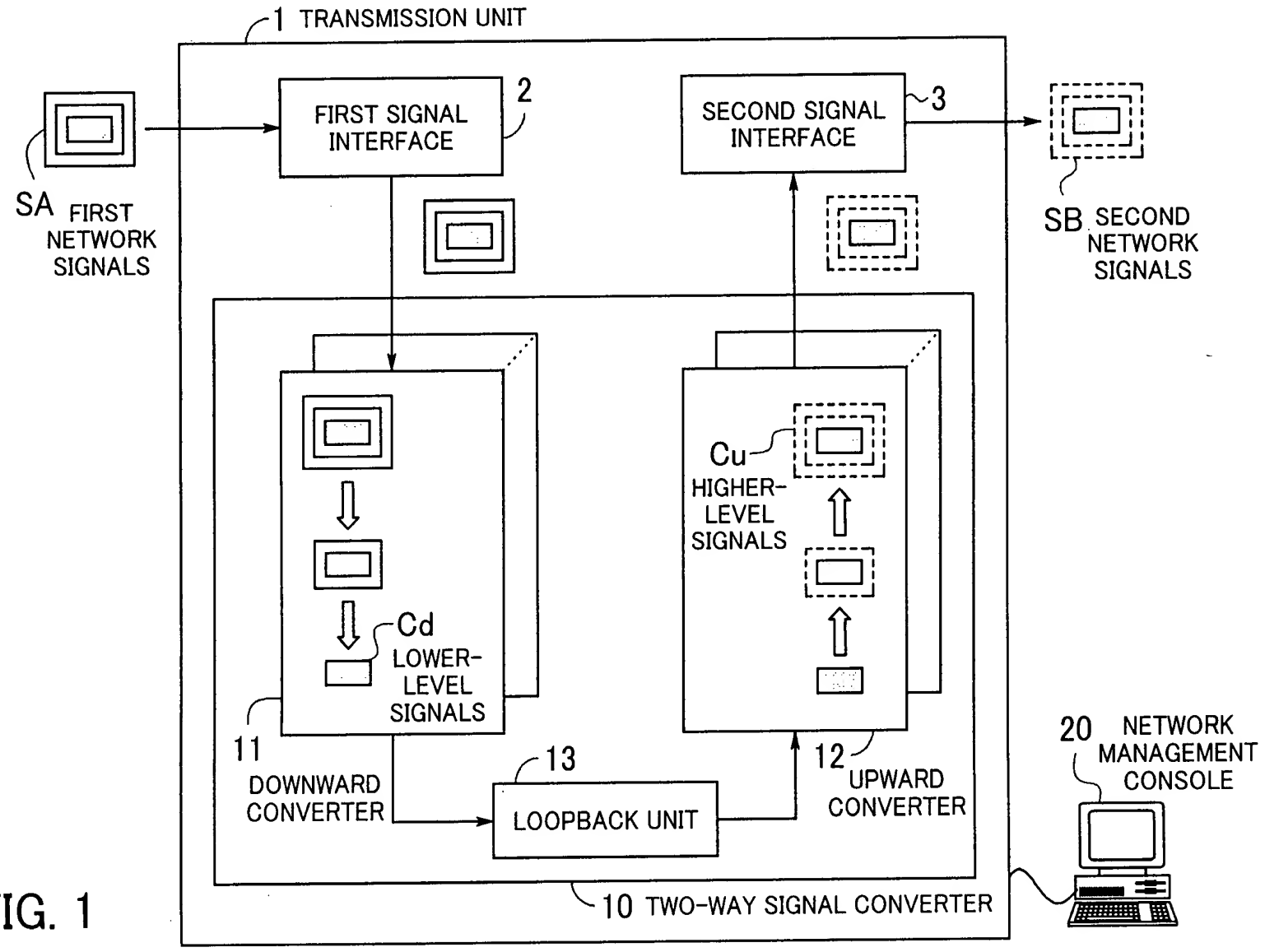

FIG. 1

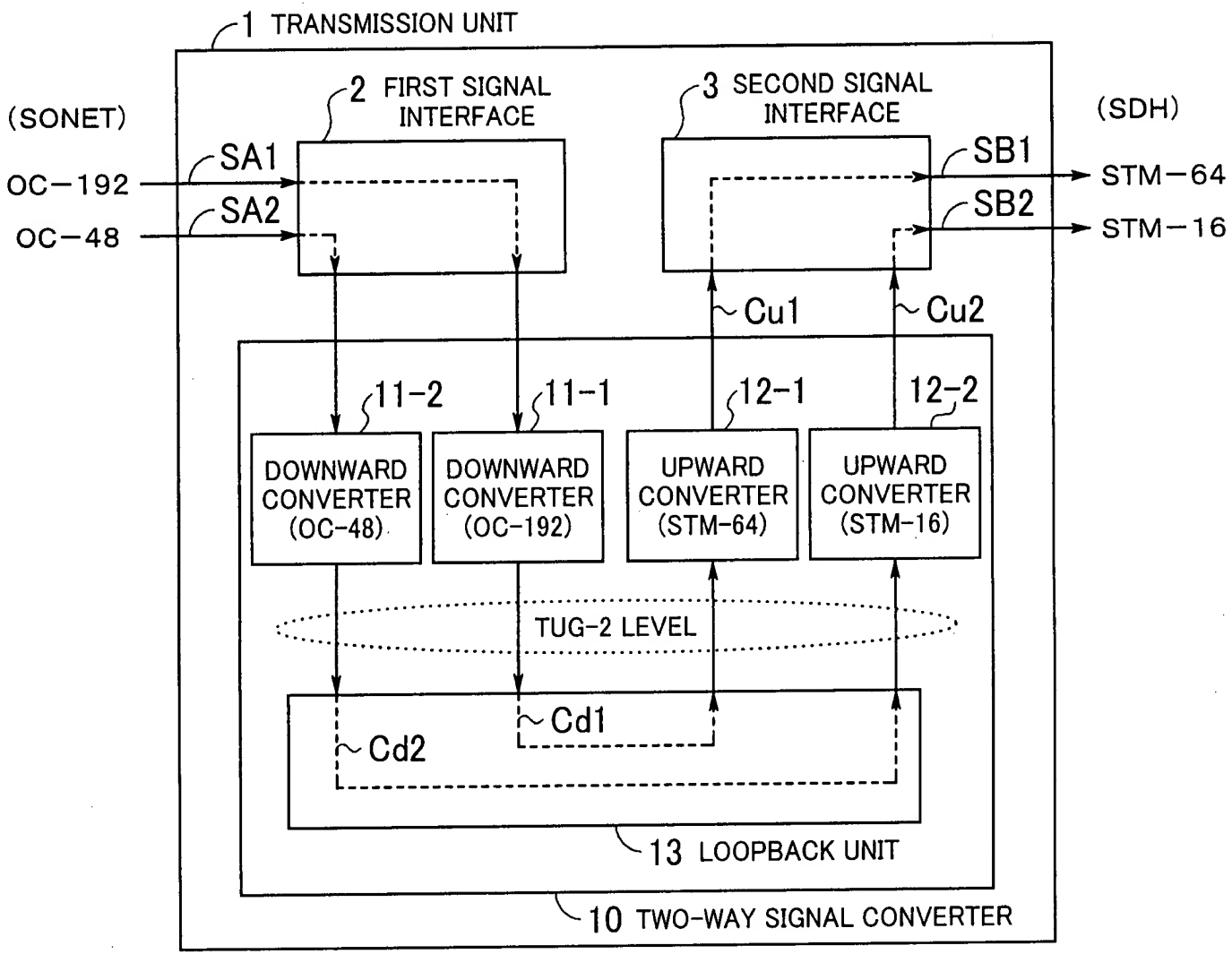
1 TRANSMISSION UNIT
(SONET)
OC−192
OC−48
SA1
SA2
2 FIRST SIGNAL INTERFACE
3 SECOND SIGNAL INTERFACE
(SDH)
SB1
SB2
STM−64
STM−16
Cu1
Cu2
11−2
11−1
12−1
12−2
DOWNWARD CONVERTER (OC-48)
DOWNWARD CONVERTER (OC-192)
UPWARD CONVERTER (STM-64)
UPWARD CONVERTER (STM-16)
TUG-2 LEVEL
Cd1
Cd2
13 LOOPBACK UNIT
10 TWO-WAY SIGNAL CONVERTER

FIG. 2

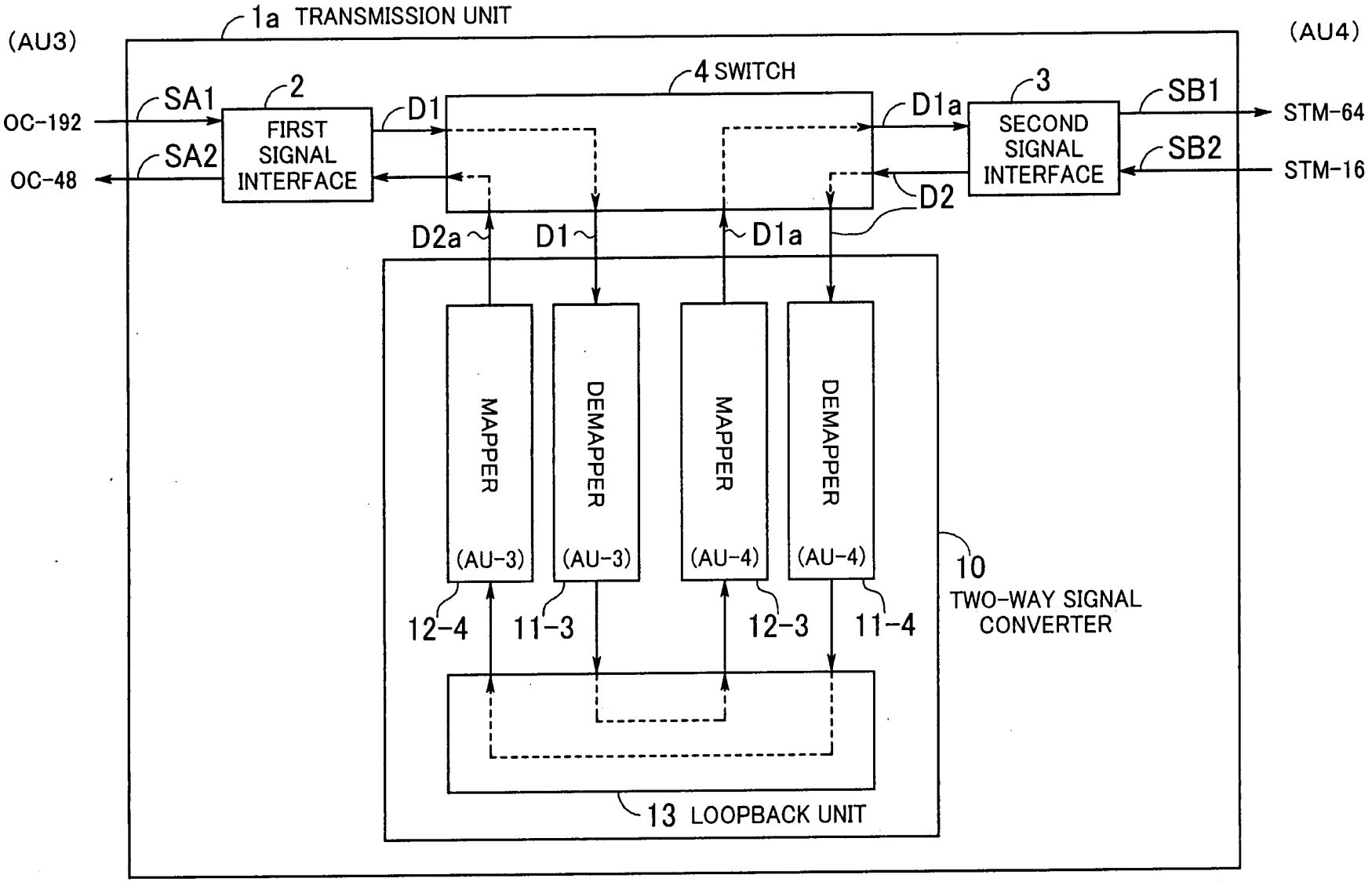
1a TRANSMISSION UNIT
(AU3)
(AU4)
4 SWITCH
SA1
2
FIRST SIGNAL INTERFACE
SA2
OC-192
OC-48
D1
D1a
3
SECOND SIGNAL INTERFACE
SB1
SB2
STM-64
STM-16
D2
D2a
D1
D1a
MAPPER
(AU-3)
DEMAPPER
(AU-3)
MAPPER
(AU-4)
DEMAPPER
(AU-4)
12-4
11-3
12-3
11-4
10
TWO-WAY SIGNAL CONVERTER
13 LOOPBACK UNIT

FIG. 3

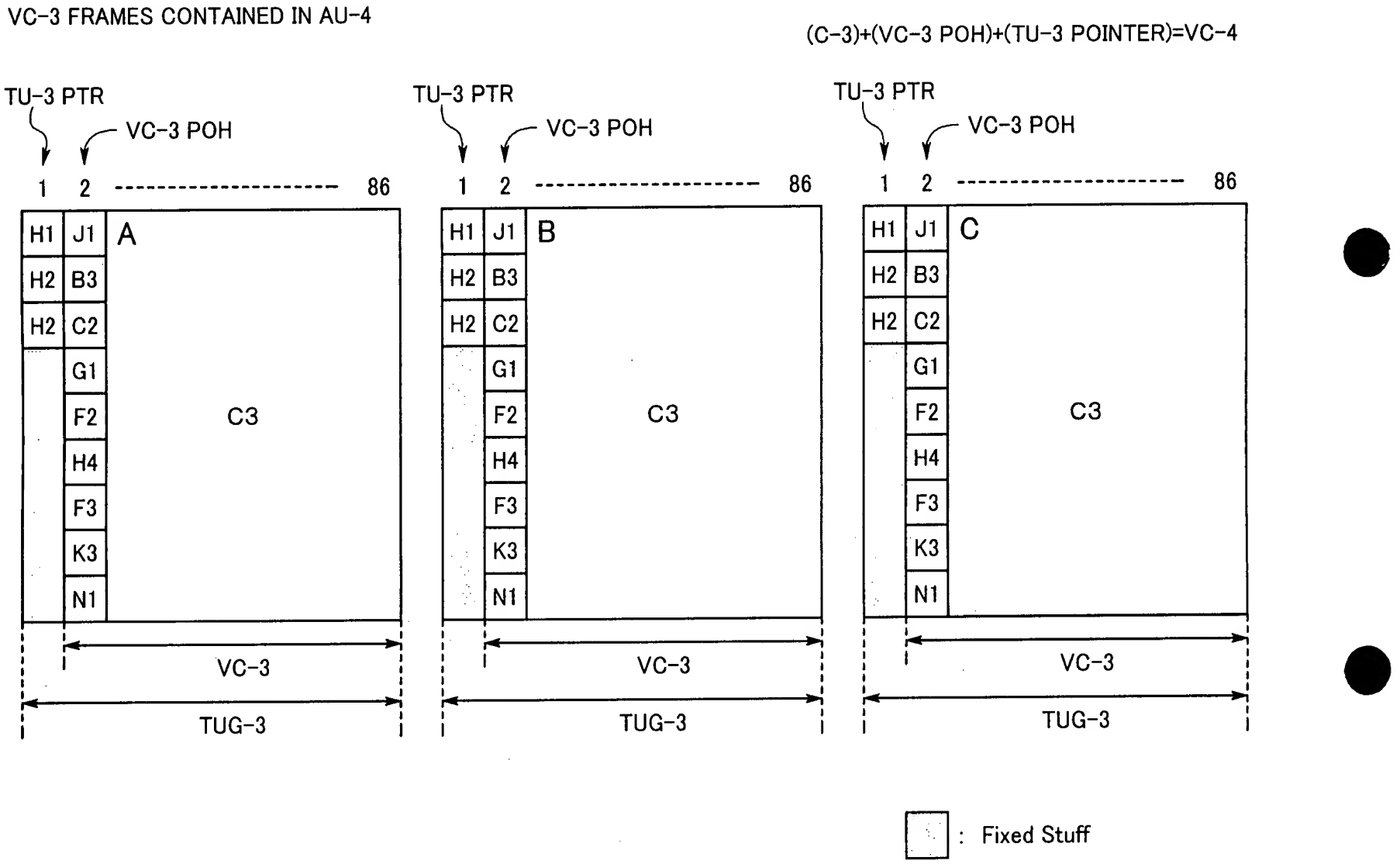
VC-3 FRAMES CONTAINED IN AU-4
(C-3)+(VC-3 POH)+(TU-3 POINTER)=VC-4
TU-3 PTR
VC-3 POH
1
2
86
H1
J1
H2
B3
H2
C2
G1
F2
H4
F3
K3
N1
A
B
C
C3
VC-3
TUG-3
: Fixed Stuff

FIG. 4

VC-4 FRAME CARRYING THREE VC-3 FRAMES TO FORM AU-4

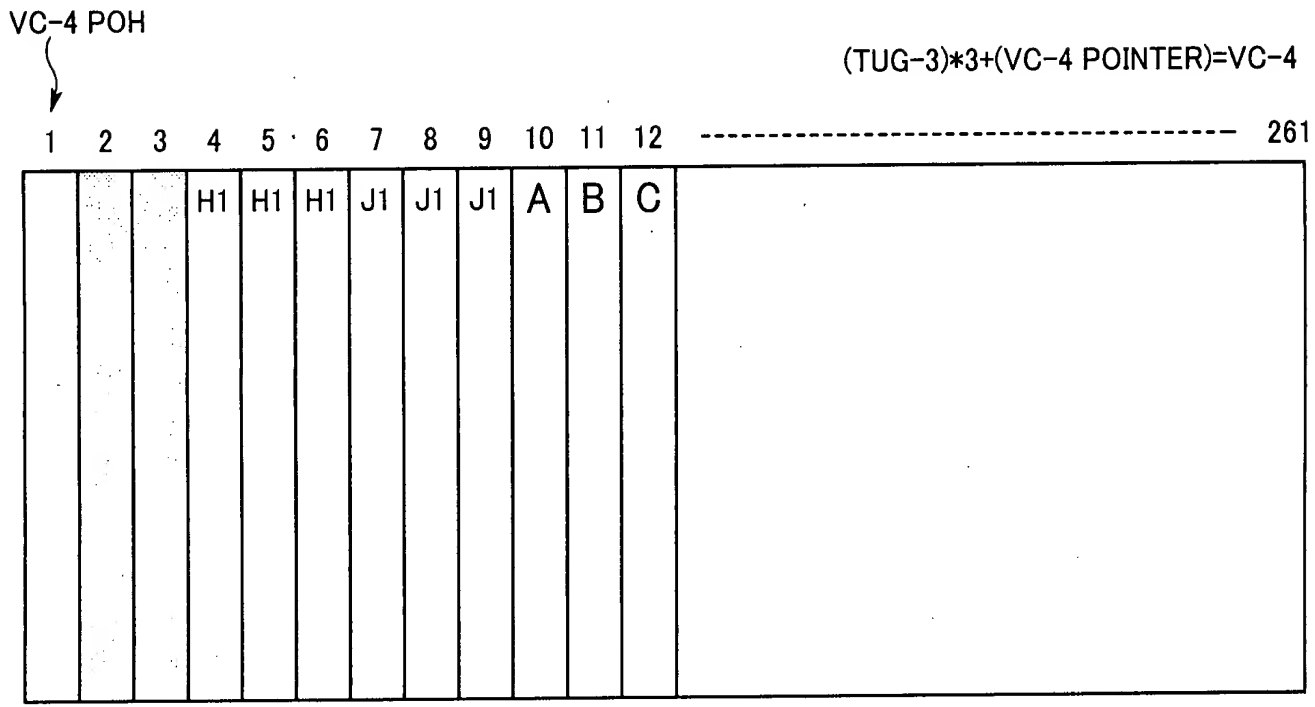

FIG. 5

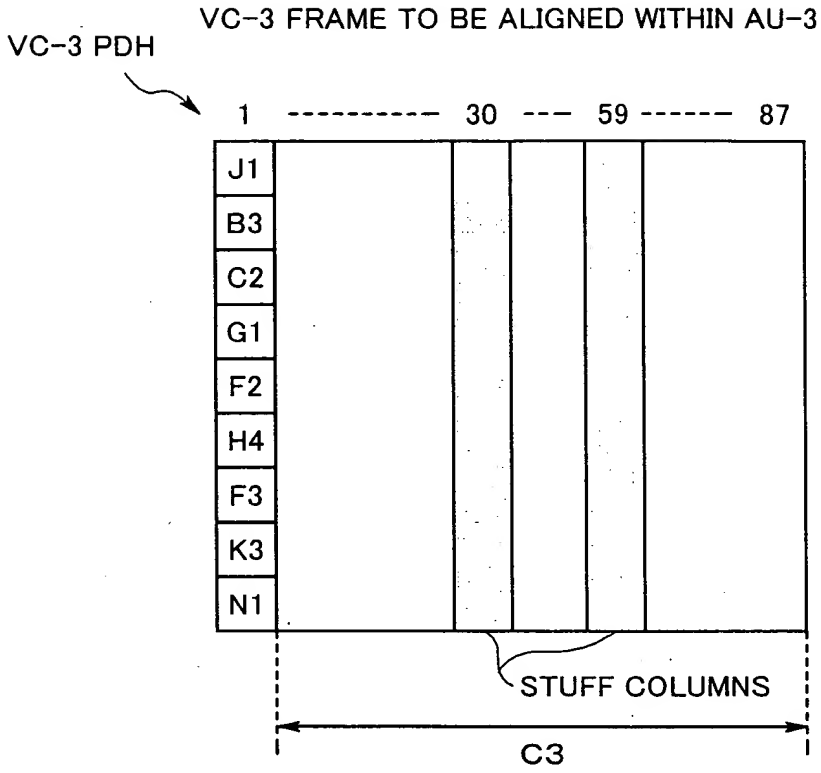
VC-3 FRAME TO BE ALIGNED WITHIN AU-3
VC-3 PDH
1
30
59
87
J1
B3
C2
G1
F2
H4
F3
K3
N1
STUFF COLUMNS
C3

FIG. 6

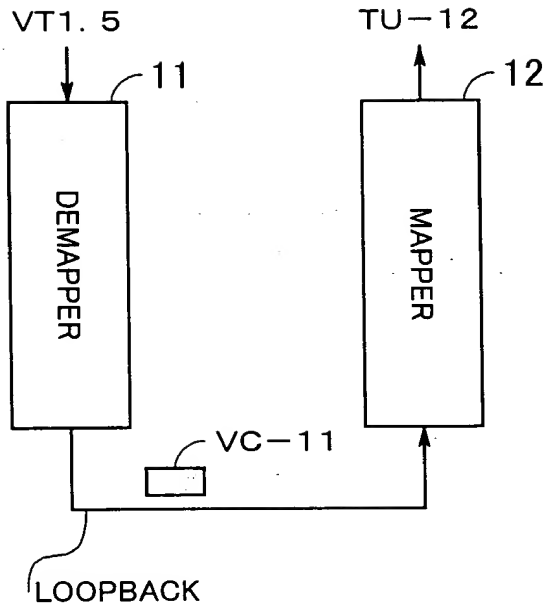

FIG. 7

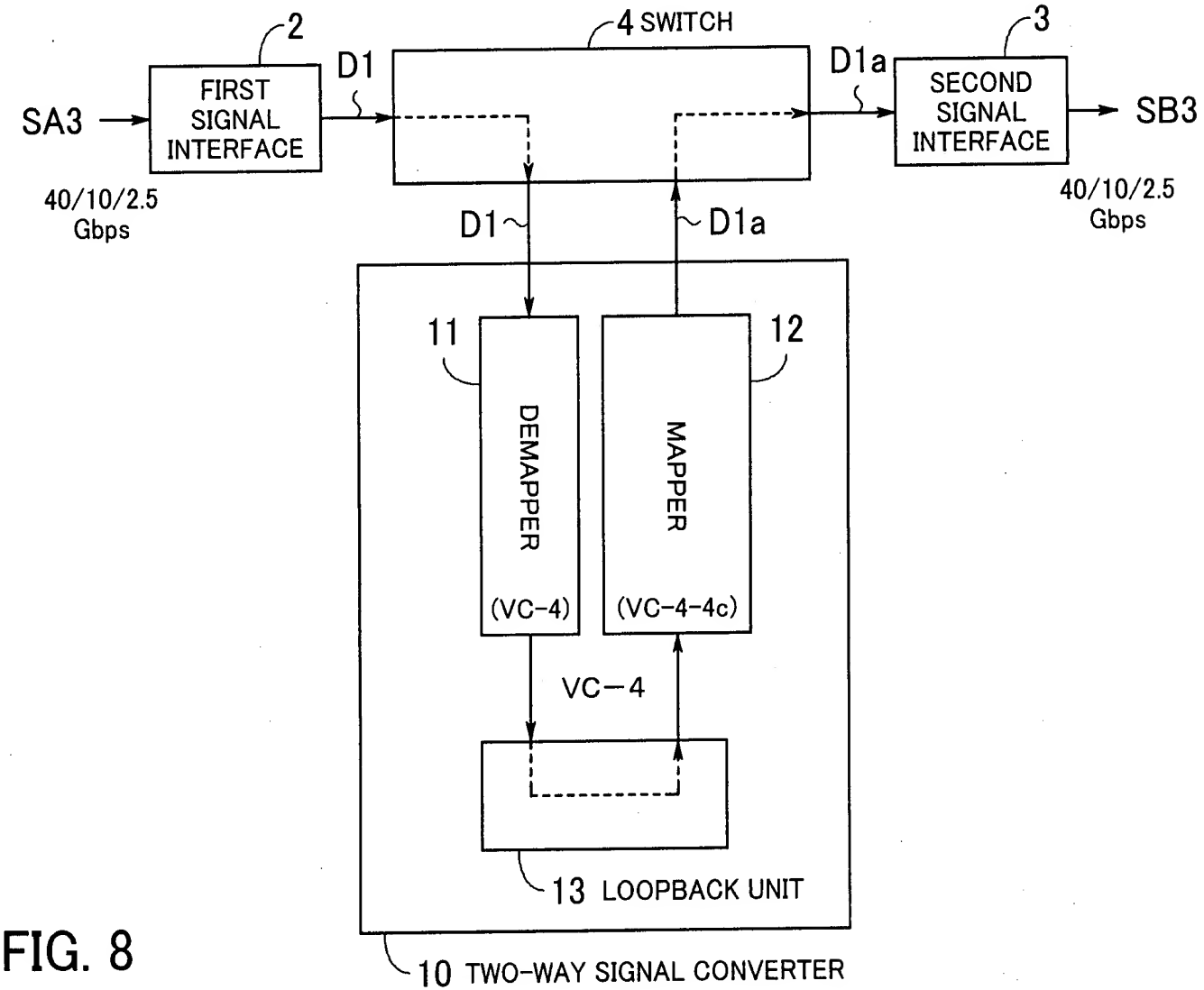
2
4 SWITCH
3
SA3
FIRST SIGNAL INTERFACE
D1
D1a
SECOND SIGNAL INTERFACE
SB3
40/10/2.5 Gbps
40/10/2.5 Gbps
D1
D1a
11
12
DEMAPPER
(VC-4)
MAPPER
(VC-4-4c)
VC−4
13 LOOPBACK UNIT
10 TWO-WAY SIGNAL CONVERTER

FIG. 8

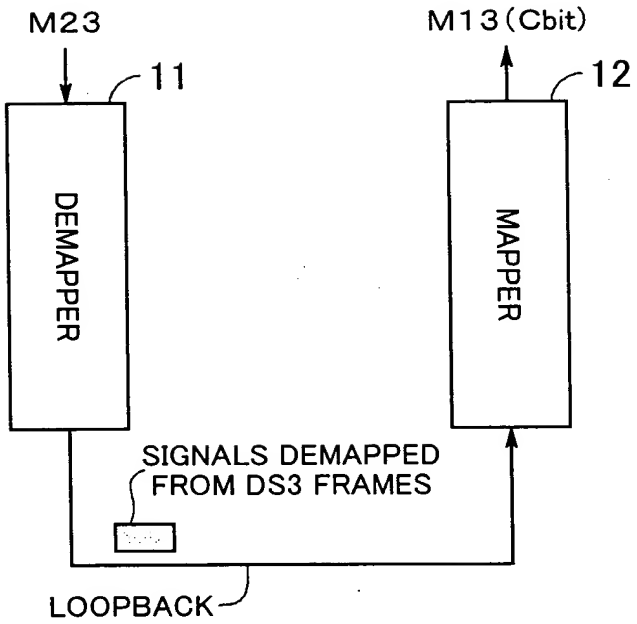
M23
11
M13 (Cbit)
12
DEMAPPER
MAPPER
SIGNALS DEMAPPED
FROM DS3 FRAMES
LOOPBACK

FIG. 9

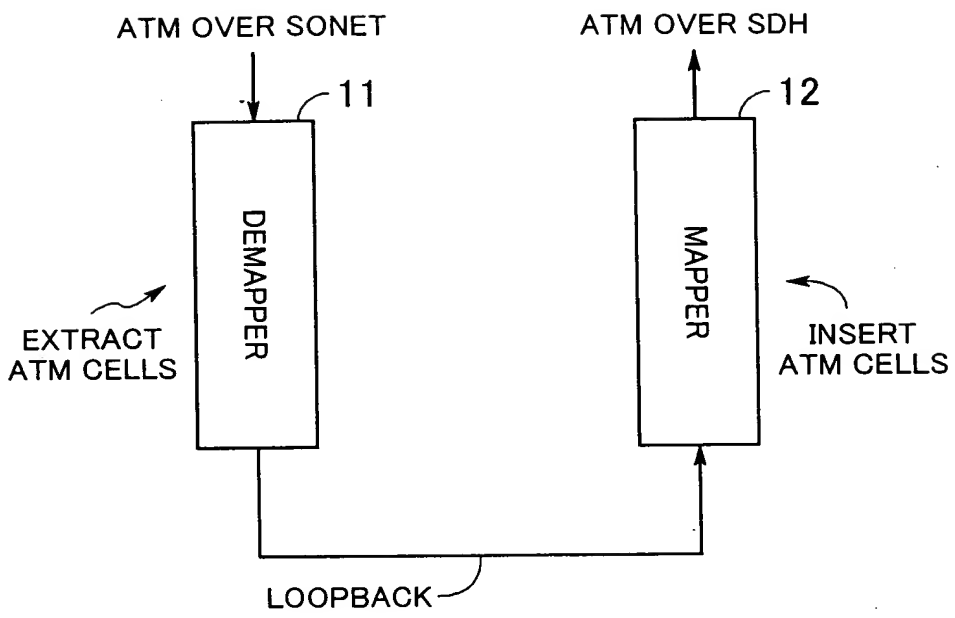
ATM OVER SONET
11
DEMAPPER
EXTRACT
ATM CELLS
ATM OVER SDH
12
MAPPER
INSERT
ATM CELLS
LOOPBACK

FIG. 10

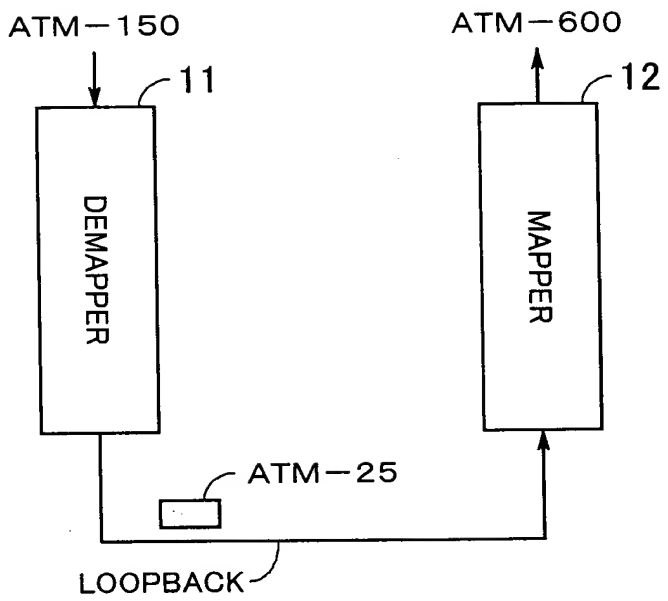

FIG. 11

05/02/2005 15:24:47 - 05/02/2005 15:24:47

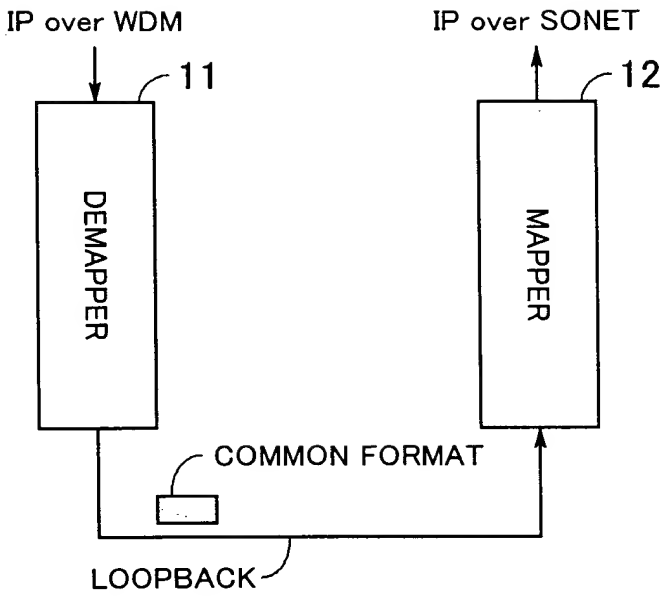

FIG. 12

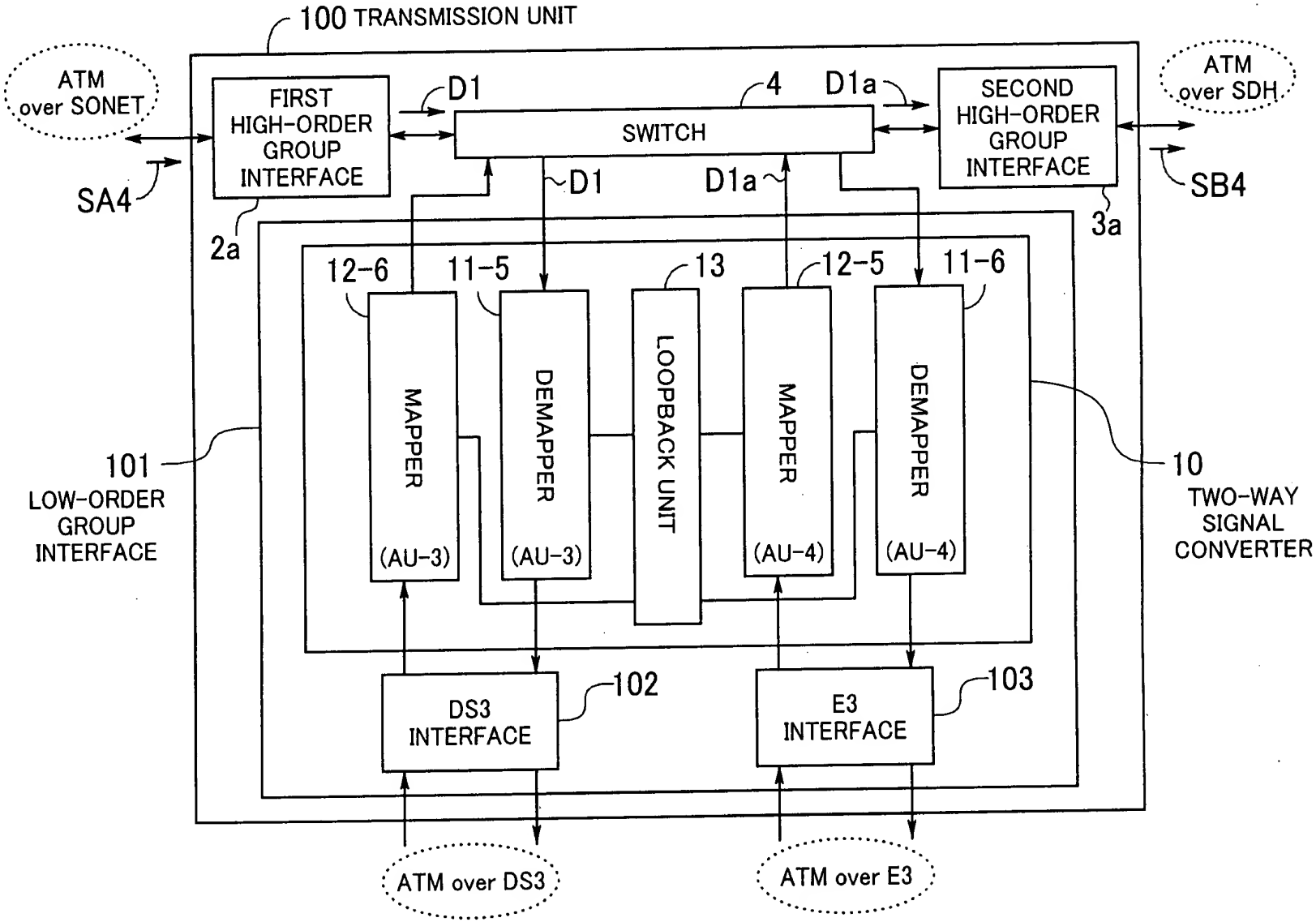
100 TRANSMISSION UNIT
ATM over SONET
FIRST HIGH-ORDER GROUP INTERFACE
D1
4
D1a
SECOND HIGH-ORDER GROUP INTERFACE
ATM over SDH
SWITCH
SA4
SB4
2a
3a
12-6
11-5
13
12-5
11-6
MAPPER (AU-3)
DEMAPPER (AU-3)
LOOPBACK UNIT
MAPPER (AU-4)
DEMAPPER (AU-4)
101
LOW-ORDER GROUP INTERFACE
10
TWO-WAY SIGNAL CONVERTER
DS3 INTERFACE
102
E3 INTERFACE
103
ATM over DS3
ATM over E3

FIG. 13

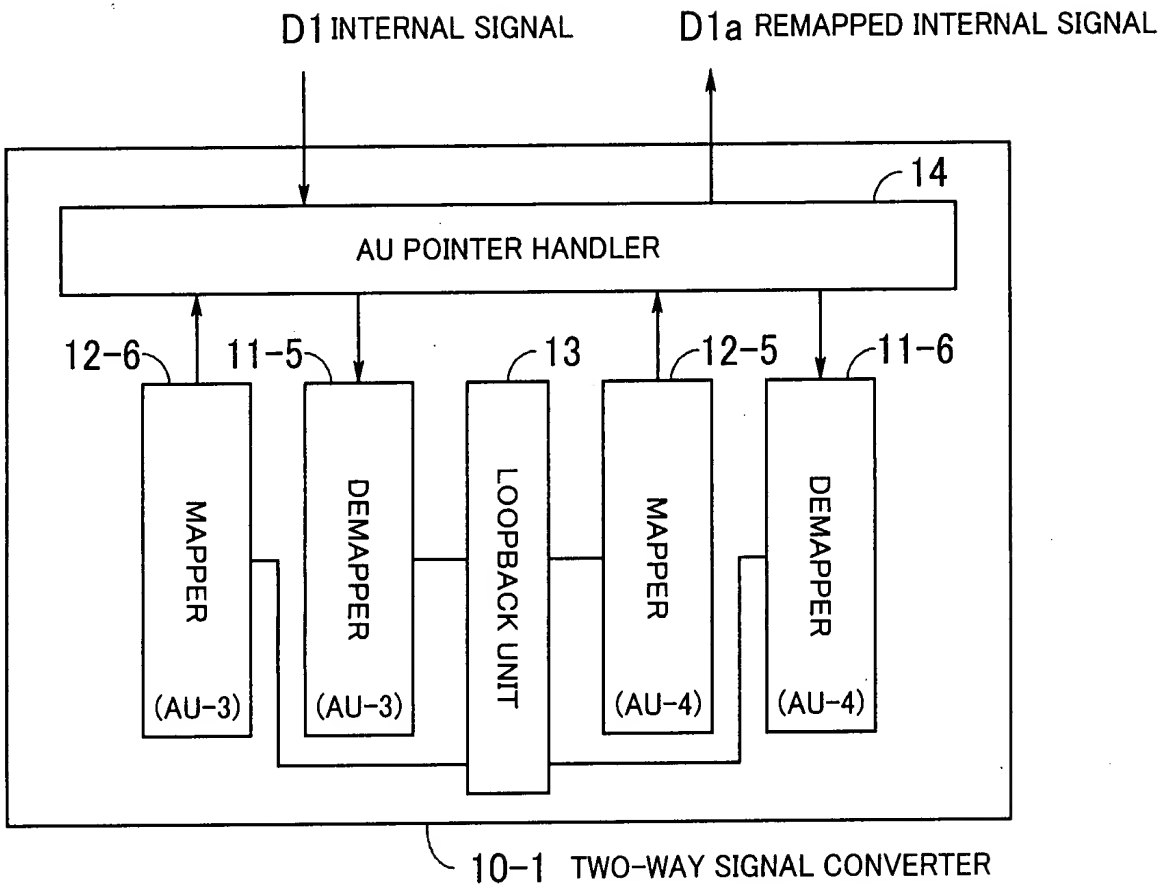
D1 INTERNAL SIGNAL
D1a REMAPPED INTERNAL SIGNAL
14
AU POINTER HANDLER
12-6
11-5
13
12-5
11-6
MAPPER
(AU-3)
DEMAPPER
(AU-3)
LOOPBACK UNIT
MAPPER
(AU-4)
DEMAPPER
(AU-4)
10-1 TWO-WAY SIGNAL CONVERTER

FIG. 14

0950530 - 4070906

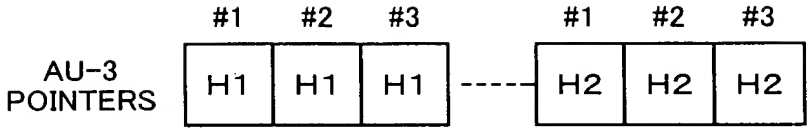

FIG. 15

09/30/2005, EAST Version: 2.0.3.0

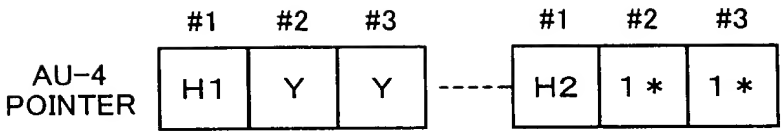

FIG. 16

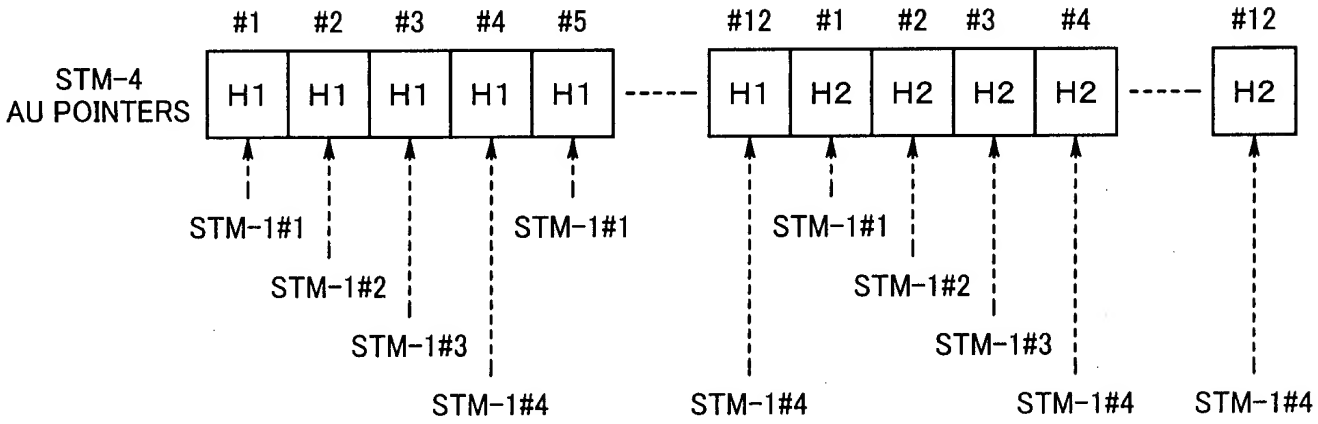
#1
#2
#3
#4
#5
#12
#1
#2
#3
#4
#12
STM-4
AU POINTERS
H1
H1
H1
H1
H1
H1
H2
H2
H2
H2
H2
STM-1#1
STM-1#2
STM-1#3
STM-1#4
STM-1#1
STM-1#4
STM-1#1
STM-1#2
STM-1#3
STM-1#4
STM-1#4

FIG. 17

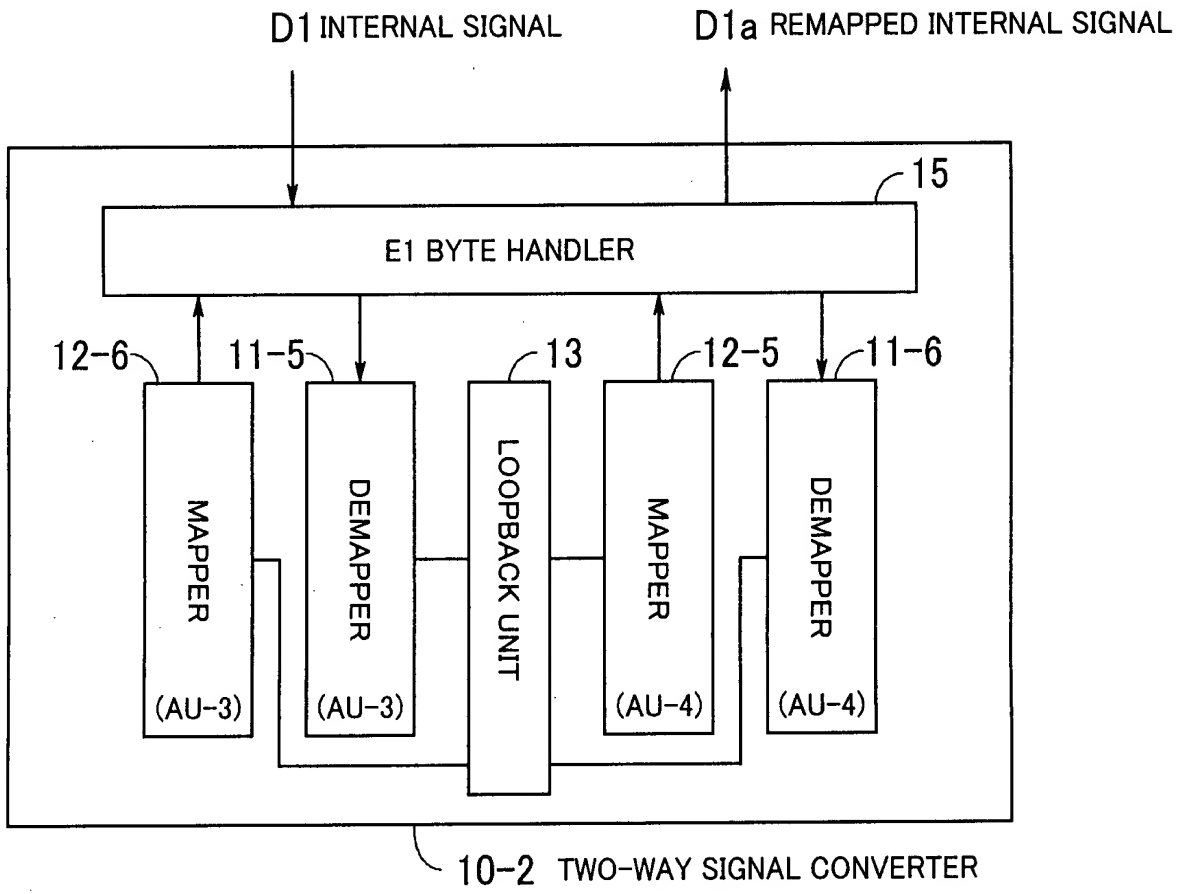
D1 INTERNAL SIGNAL
D1a REMAPPED INTERNAL SIGNAL
15
E1 BYTE HANDLER
12-6
11-5
13
12-5
11-6
MAPPER
(AU-3)
DEMAPPER
(AU-3)
LOOPBACK UNIT
MAPPER
(AU-4)
DEMAPPER
(AU-4)
10-2 TWO-WAY SIGNAL CONVERTER

FIG. 18

STM-4 FRAME OVERHEAD FORMAT USED INSIDE THE UNIT

#1	#2	#3	#12	#1	#2	#3	#12	#1	#2	#3	#12
A1	A1	A1	A1	A2	A2	A2	A2	—	—	—	—
B1	—	—	—	E1	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—	—	—	—	—
H1	H1	H1	H1	H2	H2	H2	H2	H3	H3	H3	H3
—	—	—	—	—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—	—	—	—	—

— :ALL 0

FIG. 19

BIT#	DEFINITION	STATE
1, 2	UNUSED	0
3	AU-4-16c (STS-48c)	1: CONCATENATED
4	AU-4-4c (STS-12c)	1: CONCATENATED
5	AU-4(STS-3c) #4	1: CONCATENATED
6	AU-4(STS-3c) #3	1: CONCATENATED
7	AU-4(STS-3c) #2	1: CONCATENATED
8	AU-4(STS-3c) #1	1: CONCATENATED

FIG. 20

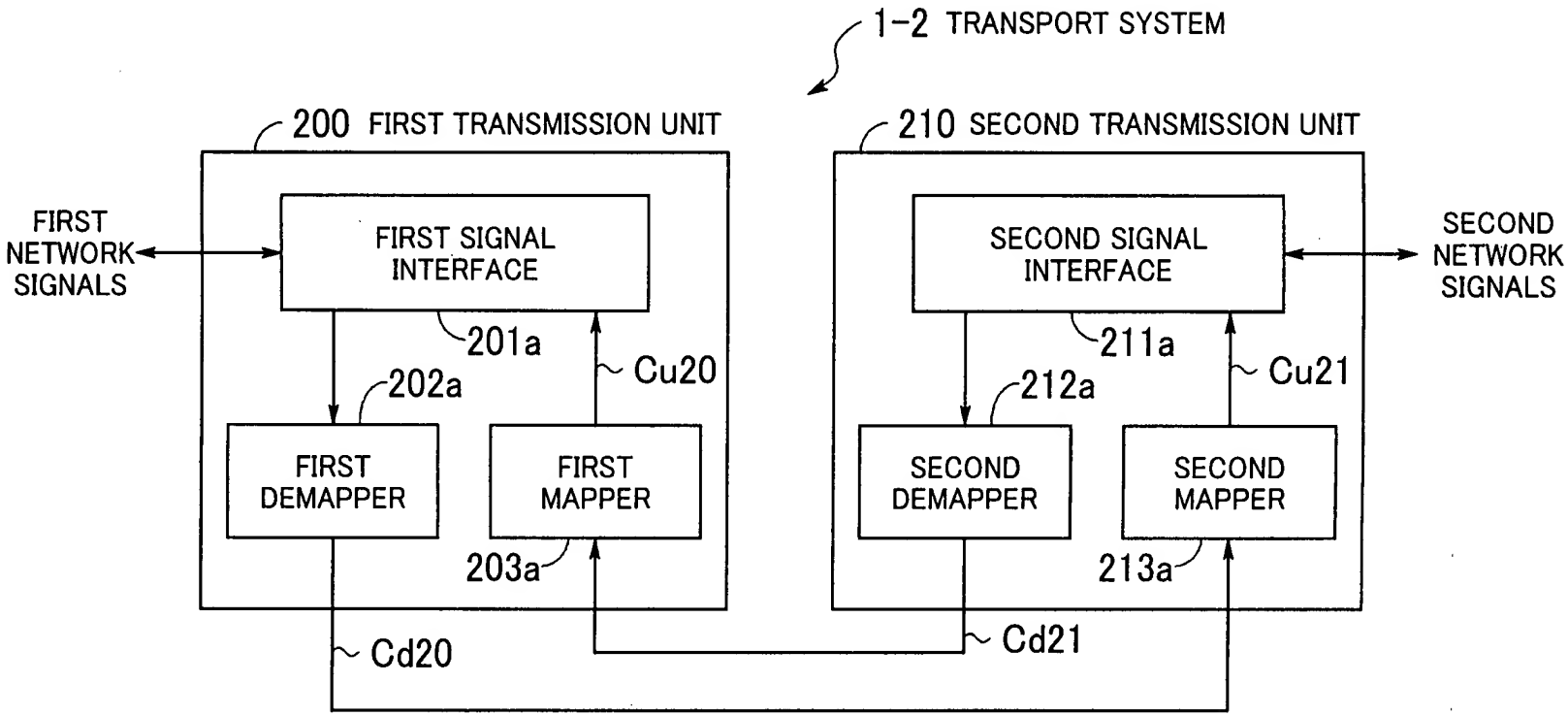
1-2 TRANSPORT SYSTEM
200 FIRST TRANSMISSION UNIT
210 SECOND TRANSMISSION UNIT
FIRST NETWORK SIGNALS
FIRST SIGNAL INTERFACE
SECOND SIGNAL INTERFACE
SECOND NETWORK SIGNALS
201a
211a
202a
212a
Cu20
Cu21
FIRST DEMAPPER
FIRST MAPPER
SECOND DEMAPPER
SECOND MAPPER
203a
213a
Cd20
Cd21

FIG. 21

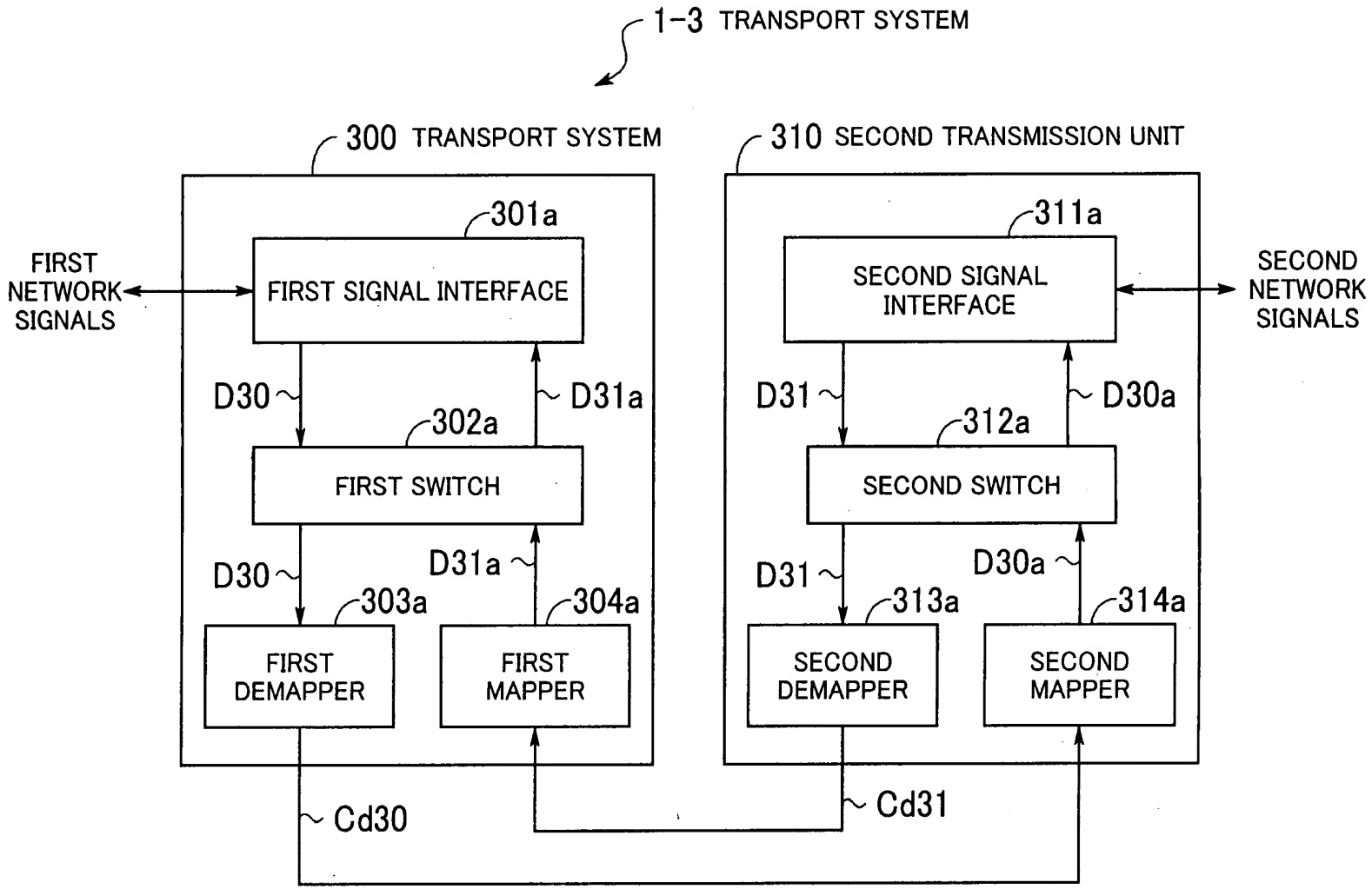
1-3 TRANSPORT SYSTEM
300 TRANSPORT SYSTEM
310 SECOND TRANSMISSION UNIT
301a
311a
FIRST NETWORK SIGNALS
FIRST SIGNAL INTERFACE
SECOND SIGNAL INTERFACE
SECOND NETWORK SIGNALS
D30
D31a
D31
D30a
302a
312a
FIRST SWITCH
SECOND SWITCH
D30
D31a
D31
D30a
303a
304a
313a
314a
FIRST DEMAPPER
FIRST MAPPER
SECOND DEMAPPER
SECOND MAPPER
Cd30
Cd31

FIG. 22

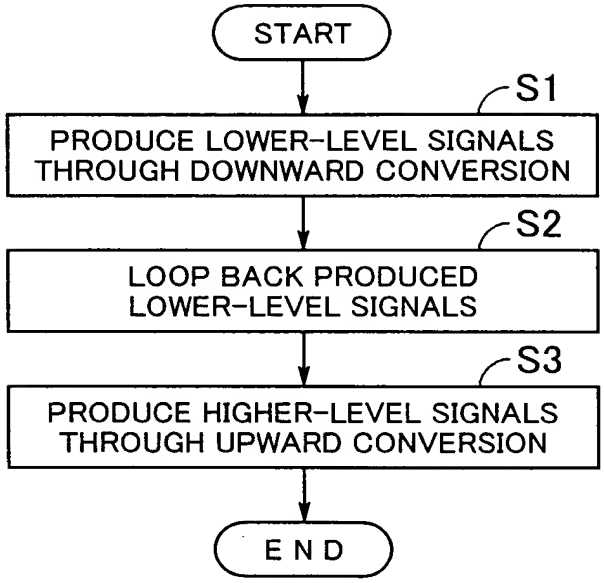
START
S1
PRODUCE LOWER-LEVEL SIGNALS THROUGH DOWNWARD CONVERSION
S2
LOOP BACK PRODUCED LOWER-LEVEL SIGNALS
S3
PRODUCE HIGHER-LEVEL SIGNALS THROUGH UPWARD CONVERSION
END

FIG. 23

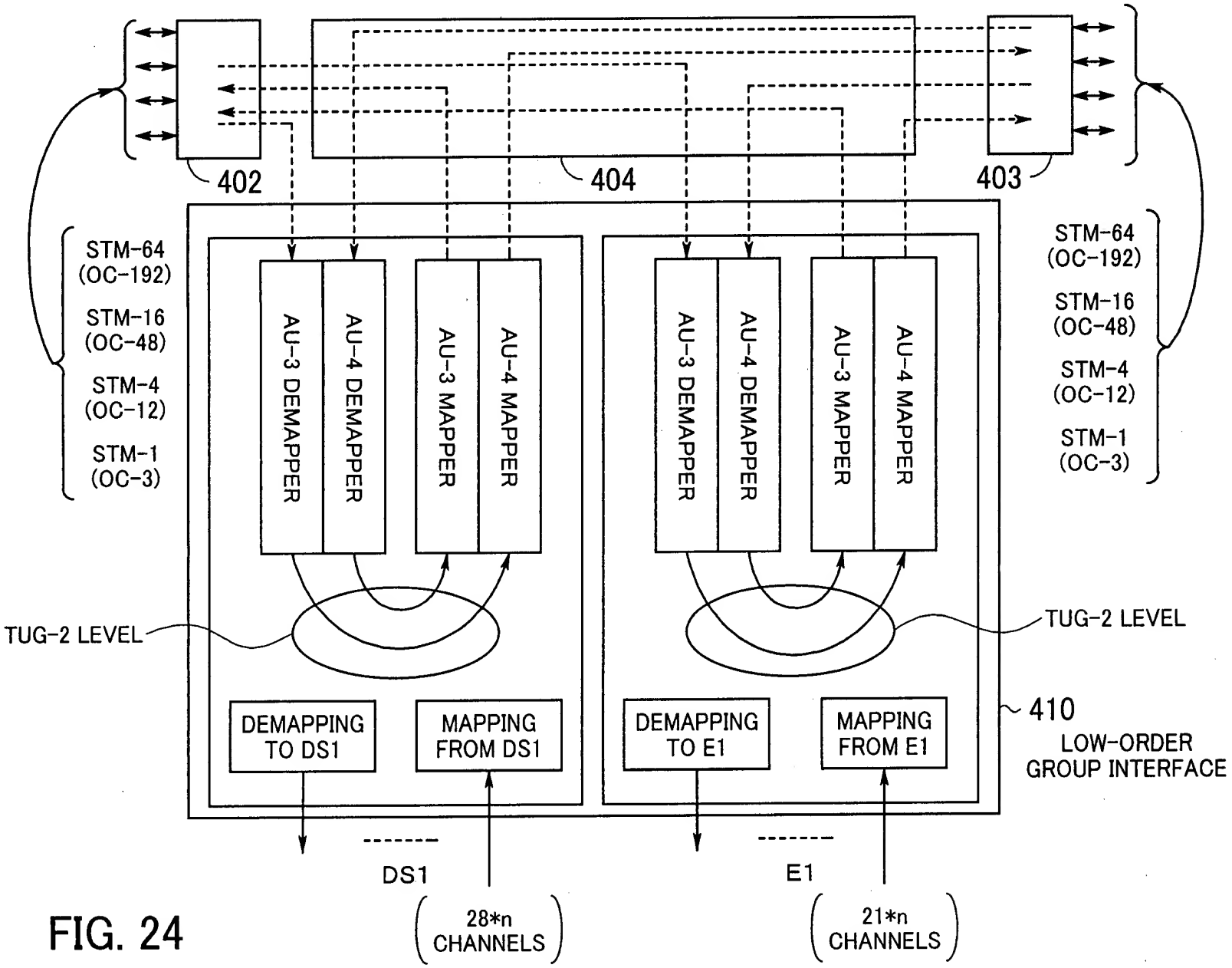
402
404
403
STM-64
(OC-192)
STM-16
(OC-48)
STM-4
(OC-12)
STM-1
(OC-3)
AU-3 DEMAPPER
AU-4 DEMAPPER
AU-3 MAPPER
AU-4 MAPPER
AU-3 DEMAPPER
AU-4 DEMAPPER
AU-3 MAPPER
AU-4 MAPPER
STM-64
(OC-192)
STM-16
(OC-48)
STM-4
(OC-12)
STM-1
(OC-3)
TUG-2 LEVEL
TUG-2 LEVEL
DEMAPPING
TO DS1
MAPPING
FROM DS1
DEMAPPING
TO E1
MAPPING
FROM E1
410
LOW-ORDER
GROUP INTERFACE
DS1
E1
28*n
CHANNELS
21*n
CHANNELS

FIG. 24

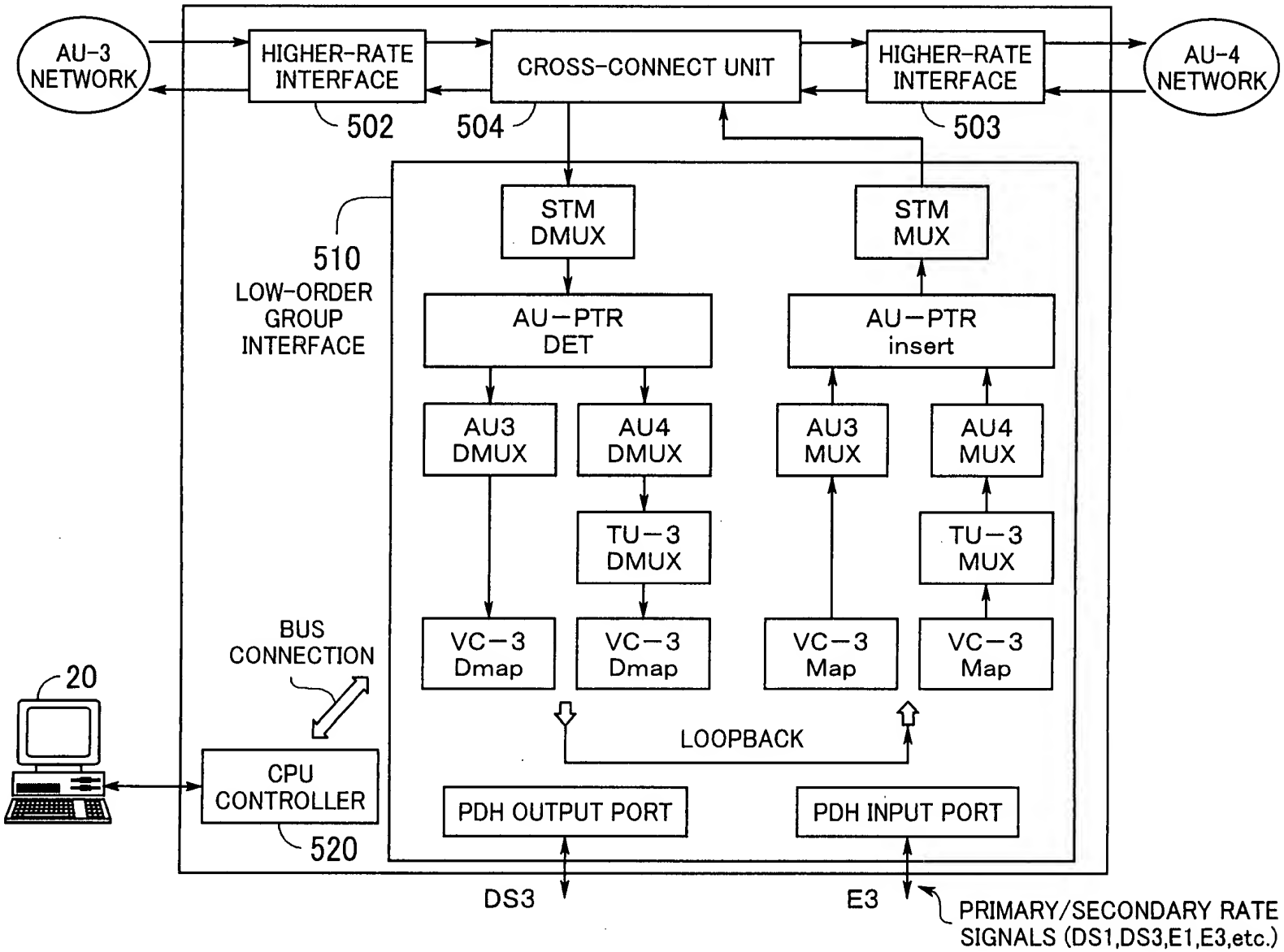
AU-3 NETWORK
HIGHER-RATE INTERFACE
502
CROSS-CONNECT UNIT
504
HIGHER-RATE INTERFACE
503
AU-4 NETWORK
510
LOW-ORDER GROUP INTERFACE
STM DMUX
STM MUX
AU-PTR DET
AU-PTR insert
AU3 DMUX
AU4 DMUX
AU3 MUX
AU4 MUX
TU-3 DMUX
TU-3 MUX
VC-3 Dmap
VC-3 Dmap
VC-3 Map
VC-3 Map
BUS CONNECTION
LOOPBACK
20
CPU CONTROLLER
520
PDH OUTPUT PORT
PDH INPUT PORT
DS3
E3
PRIMARY/SECONDARY RATE SIGNALS (DS1,DS3,E1,E3,etc.)

FIG. 25

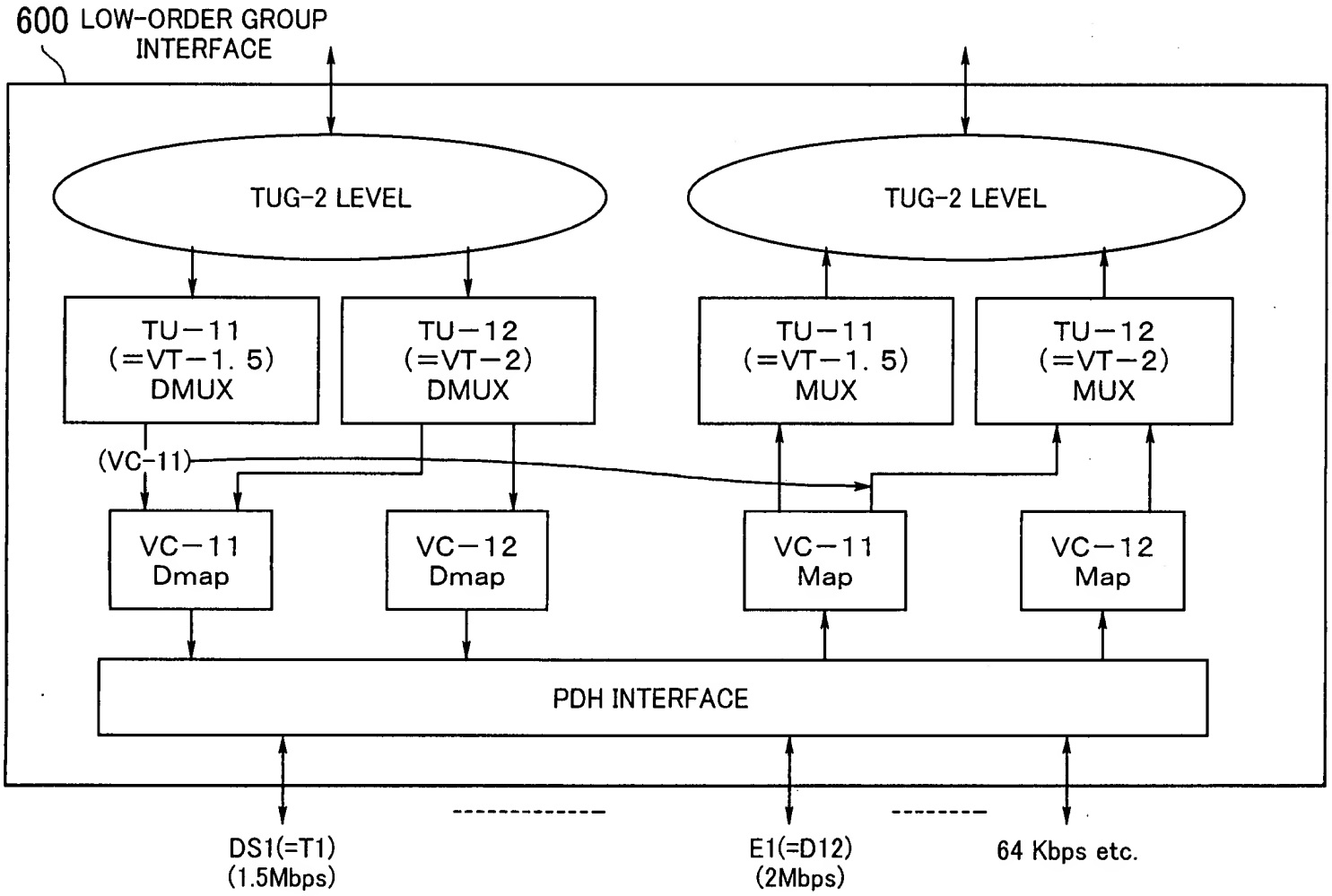
600 LOW-ORDER GROUP INTERFACE
TUG-2 LEVEL
TUG-2 LEVEL
TU−11 (=VT−1. 5) DMUX
TU−12 (=VT−2) DMUX
TU−11 (=VT−1. 5) MUX
TU−12 (=VT−2) MUX
(VC-11)
VC−11 Dmap
VC−12 Dmap
VC−11 Map
VC−12 Map
PDH INTERFACE
DS1(=T1) (1.5Mbps)
E1(=D12) (2Mbps)
64 Kbps etc.

FIG. 26

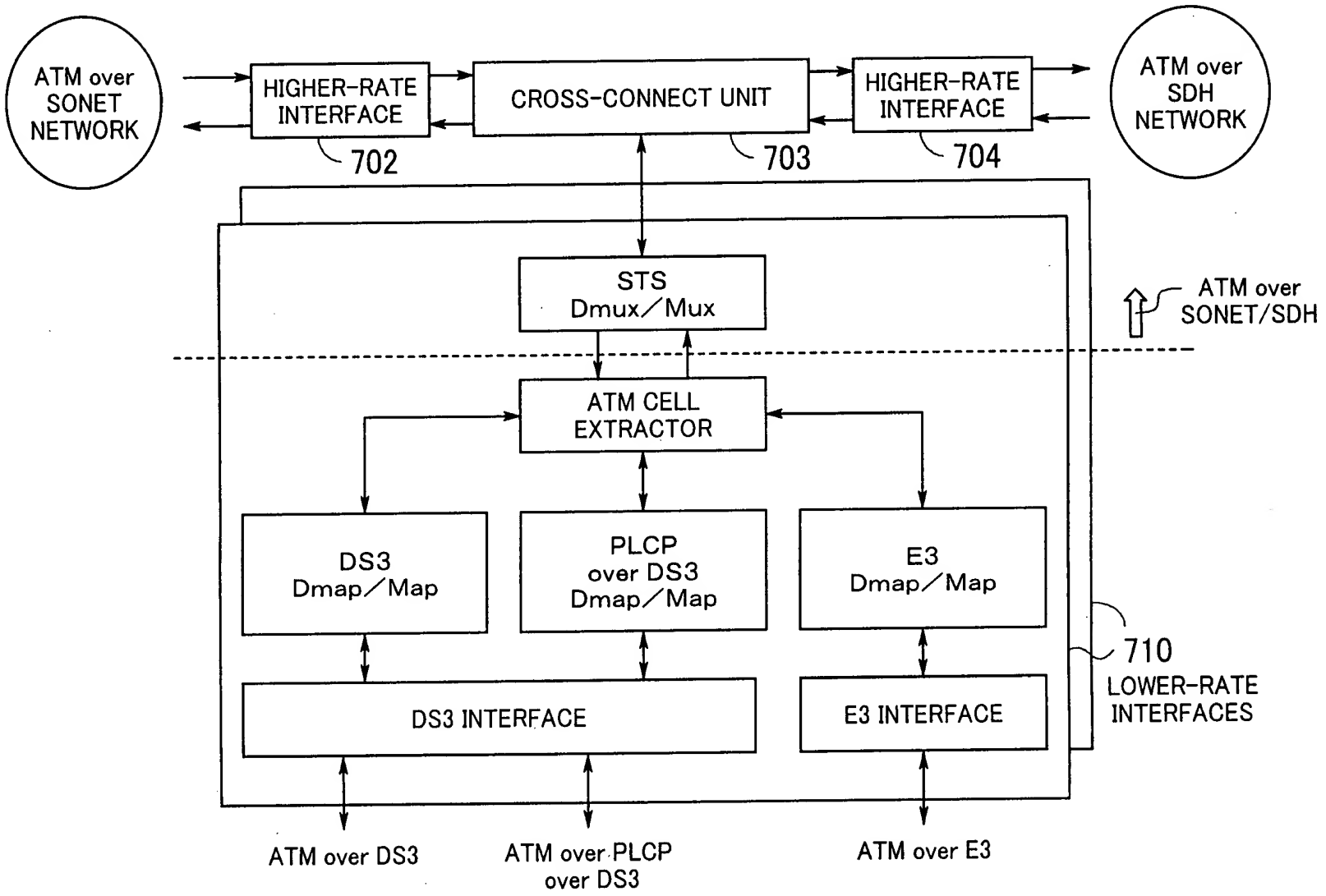
ATM over SONET NETWORK
HIGHER-RATE INTERFACE
CROSS-CONNECT UNIT
HIGHER-RATE INTERFACE
ATM over SDH NETWORK
702
703
704
STS Dmux/Mux
ATM over SONET/SDH
ATM CELL EXTRACTOR
DS3 Dmap/Map
PLCP over DS3 Dmap/Map
E3 Dmap/Map
710
LOWER-RATE INTERFACES
DS3 INTERFACE
E3 INTERFACE
ATM over DS3
ATM over PLCP over DS3
ATM over E3

FIG. 27

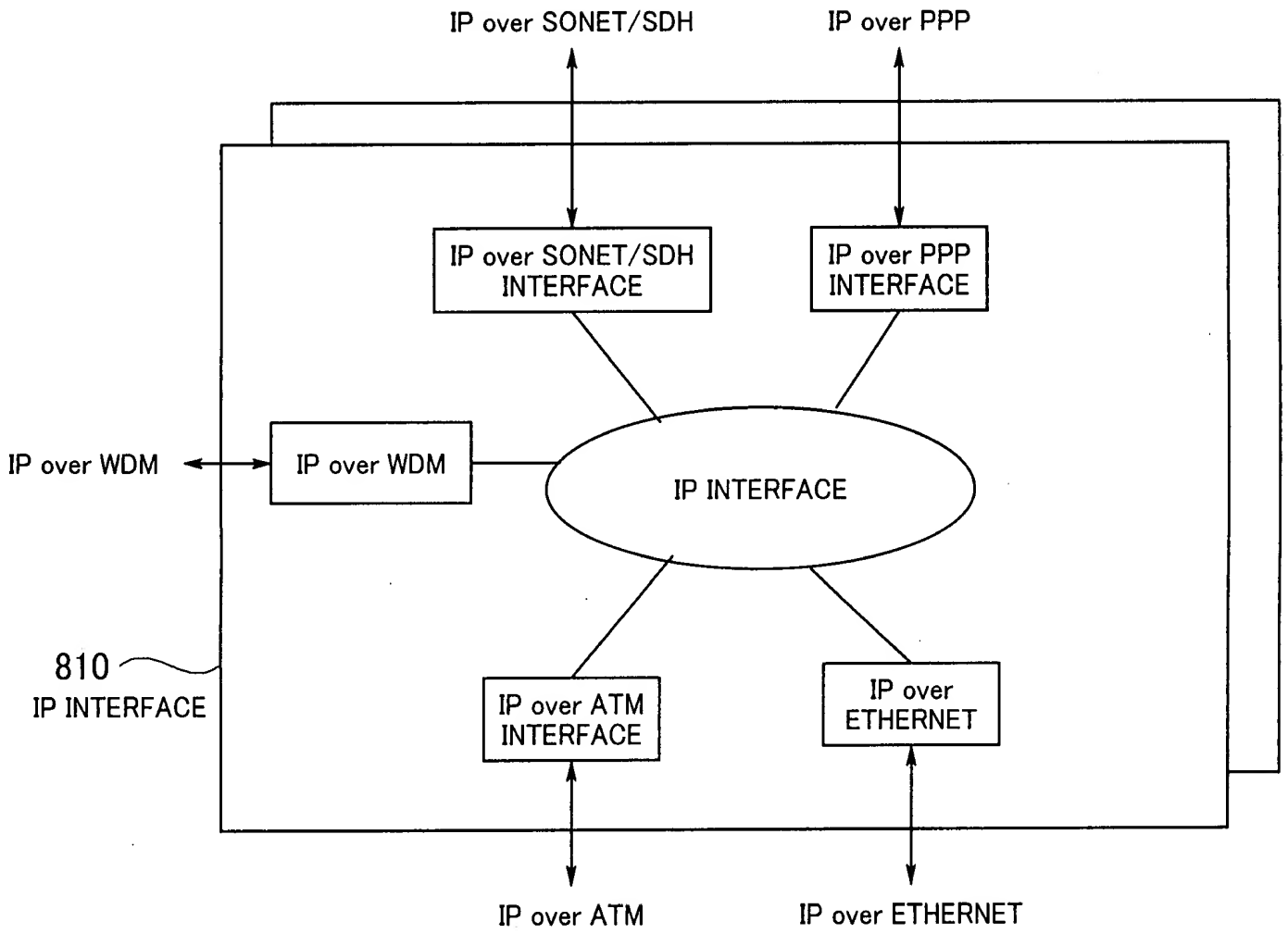
IP over SONET/SDH
IP over PPP
IP over SONET/SDH INTERFACE
IP over PPP INTERFACE
IP over WDM
IP over WDM
IP INTERFACE
810
IP INTERFACE
IP over ATM INTERFACE
IP over ETHERNET
IP over ATM
IP over ETHERNET

FIG. 28